REMARKS/ARGUMENTS:

Claims 40, 41, 47, 60, 61, 63-74, 76-79 and 81-84 are now pending in the application for consideration. Claims 42-46, 48, and 75 have been cancelled; claims 40, 62-64, 76 and 80 have been amended and new claims 82-84 have been added.

The courtesy of an interview with the Examiner by one of the inventors, Dr. J. Lyding and the undersigned attorney on April 10, 2003 is greatly appreciated; no agreement was reached regarding the outstanding rejections contained in the Office Action mailed October 29, 2002.

Claim Rejections – 35 US 112

The Examiner has maintained the rejection of claims 66-74 under 35 US 112, first paragraph, asserting "Applicants must show that the claimed concentration necessarily results from what is described in application S/N 08/586,411 ..." (emphasis in the original). It is believed this condition has been fulfilled. At page 4 lines 17-19 of the Office Action, it is stated "The examiner finds that the example set forth therein [pages 14-18 of the '411 application] only establishes a deuterium anneal that occurs at some point after the gate electrodes of the NMOS transistors are formed – not post-metalization or after the metal contacts are formed." (Emphasis in the original.) With respect, it is maintained that the Examiner's conclusion is incorrect. The annealing of transistor structures under process parameters described at pages 14-18 of the '411 application is identical to those described in *Applied Physics Letters,* 68 (18), pp. 2526-2528, 29 April 1996 (Exhibit A to the affidavit of Dr. Joseph Lyding dated February 6, 2001, and in both cases the transistor structures are identical *Applied Physics Letters* page 2526, paragraph bridging the left and right columns, and Reference No. 6 to that publication, and the '411 application at page 14, lines 15-19, and the post-anneal tests and the test results are identically the same – see '411 application page 17, line 1 to page 18, line 10 and *Applied Physics Letters,* page 2526, right column, first complete paragraph and paragraph bridging pages 2526 and 2527, including the identicality of the gm (transconductance) and threshold voltage (Vth) with time plots shown in Figs. 2 and 3 of the '411 application and Figs. 1 and 2 of *Applied Physics Letters.* Then, in the final paragraph of page 2527 of *Applied Physics Letters* it is stated, "*...the replacement of hydrogen with deuterium during the final wafer sintering process results in substantially reduced susceptibility to hot electron degradation effects.*" (Emphasis added). The deuterium annealing process as described in the '411 application at

pages 14-18, just as the identical process described in *Applied* Physics, thus occurred after metal contact formation on the transistors, consistent with the disclosure of the Ference article. Consequently, it is believed Applicants have made the requisite showing that the concentration of deuterium in the gate oxide that is described by Ference is an inherent property of Applicants' written description and that claims 66-74 are supported by the specification of the '411 application in compliance with 35 US 112. Withdrawal of this ground of rejection of claims 66-74 is believed in order and is respectfully requested, as well as initiation of an interference with U.S. Patent 6,023,093 as previously requested.

Claim Rejections – 35 US 103

Before addressing the specific rejections of claims based on combinations of various references, the disclosure of lack of pertinence of PCT International Application WO 94/19829 (Lisenker) will be discussed.

Lisenker's disclosure emphasizes employment of deuterium during processing steps "before, during and/or after formation of a device oxide layer" (p. 6, lines 10-14; see also p. 5, lines 6-14 and p. 8, line 29 to page 9, line 4). The Office Action appears to imply that post contact annealing of semiconductor devices in deuterium would have been obvious based on Lisenker's disclosure, if a speculatively expansive reading is given of a prefatory sentence at Lisenker, page 8, lines 29 and 30: "The present invention can be implemented throughout the VLSI fabrication procedure." But this sentence may not arbitrarily be extracted and considered alone, ignoring the context of the remainder of Lisenker's teaching. In the very next sentence, Lisenker qualifies that assertion by stating "A typical fabrication procedure will include various doping, etching, annealing, deposition, cleaning, passivation, and oxidation steps." This is consistent with and reinforces the above quoted statements by Lisenker on pages 5 and 6 of his specification. It is in this context that Lisenker would have been considered at the time of the present invention, unprejudiced by the teaching presented in the present application. Significantly, there is no mention or suggestion of contact formation or metalization by Lisenker.

Further, Lisenker must be considered not in isolation but in the context of the prior art at the time of the invention of the present application. Another cited reference, *IEEE Transactions on Nuclear Science*, Vol. 39, No. 6, December 1992, pp. 2220-2229 (Saks), although, for reasons

discussed below, not considered pertinent to the invention claimed in this application, does include disclosure relevant to evaluation of Lisenker. Saks investigated the effects of ionizing radiation on MOSFET gate oxides into which deuterium and hydrogen had been introduced "after definition of the polysilicon gates and implantation of the N+ source/drains" (P. 2221, left col.). Saks noted an increase in trap build-up time in the deuterium annealed oxide, compared with hydrogen annealed oxide, but concluded "[b]ecause of the large +-25% experimental uncertainty, it is unclear how much of the measured variation is real." (p. 2224, right col., conclusion (1)). Subsequently (p. 2222, right column), Saks states: "One of the uncertainties in the sample fabrication procedure in this work was whether to include a 'sinter' (an anneal at 400-450°C in hydrogen), which is normally the last moderately high temperature processing step after deposition of the aluminum metalization. The purpose of the sinter is to reduce the initial interface trap density to obtain improved operating characteristics." Saks then reported, "after aluminum deposition" the ionized devices were subjected to sintering in hydrogen and deuterium, respectively and concluded – see page 2222, right column, second paragraph – "... sintering had no discernible effect on the radiation sensitivity of any of the three oxide types" (the third oxide type was a "no sinter" reference oxide). Consequently, a person of ordinary skill in the art at the time of the invention claimed in the present application, would have been likely to have disregarded Lisenker's academically based teaching based on the conclusions reached by Saks practical experimentation that (a) deuterium annealing "after definition of the polysilicon gates and implantation of the N+ source/drains", i.e. "fabrication steps in which a permanent oxide layer is being formed or treated" (Lisenker, p. 8, lines 35-37) would have little benefit compared with hydrogen annealing, and (b) would not have been motivated to use deuterium sintering after metalization based on Saks conclusion that such sintering, whether using hydrogen or deuterium, "has only minor effects" (Saks, p. 2224, right col., conclusion (3) and p. 222, right col. - discussion of Fig. 1.). In the light of these conclusions by Saks, to suggest that Lisenker's statement "The present invention can be implemented throughout the VLSI fabrication procedure" would have implied utility of post contact annealing in deuterium lacks credibility, as does Lisenker's overall theoretical dissertation.

Consequently, a person of ordinary skill in the art at the time of the invention would not have arrived at the invention claimed in any of the claims under rejection based on Lisenker

considered alone or in conjunction with any of the other references relied on in the Office Action, as will be discussed below.

Referring to the specific grounds of rejection contained in the Office Action:

- Claims 40-48, 60-65 and 75-78 have been rejected under 35 US 103 as unpatentable over US Patent 5,514,628 (Enomoto) in view of PCT International Application WO 94/19829 (Lisenker). Claims 42-46, 48, and 75 have been cancelled making the rejection moot in respect of those claims. The rejection is respectfully traversed as to claims 40, 41, 47, 60-65 and 76-78.

The Examiner's rejection is predicated on his opinion that it would have been obvious "to replace the hydrogen of post metalization step in Enomoto, with deuterium as suggested by Lisenker", based on asserted motivation that "comes from Lisenker's teaching that deuterium is superior to hydrogen for increasing device quality and reliability, and that deuterium can be substituted for hydrogen in passivation processes." This conclusory opinion refutes the Examiner's own concession that Lisenker "does not teach a deuterium annealing step that occurs after electrical contacts have been formed on a semiconductor device." Enomoto is directed to use of conventional hydrogen annealing during a testing process to detect defective memory cells in a DRAM , so that such defective cells could be replaced by redundant cells prior to device packaging. Hot carrier effects, to which Lisenker's teaching is directed, were not a significant issue in DRAMs, at least at the time of the present invention, and Lisenker would not have motivated substitution of deuterium for the well known hydrogen annealing process to stabilize device operation, used by Enomoto. Moreover, as discussed above, the teaching of Lisenker emphasizes employment of deuterium annealing "in those fabrication steps in which a permanent oxide layer is being formed or treated (Page 8, lines 35-37) and would not have suggested or motivated employment in Enomoto's process for detecting defective memory cells in an array of cells following interconnect metalization to form a DRAM integrated circuit. Withdrawal of this ground of rejection is respectfully urged.

- Claims 40-48, 60-65 and 75-81 also have been rejected under 35 US 103 as unpatentable over IEEE Transactions of Electron Devices, Vol. 41, No. 12, December

1994, pp 2369-2375 (Okazaki) in view US Patent 5,864,161 (Mitani) and Lisenker. Claims 42-46, 48, and 75 have been cancelled making the rejection moot in respect of those claims. The rejection is respectfully traversed as to claims 40, 41, 47, 60-65 and 76-81.

That Lisenker would not have motivated post contact employment of deuterium annealing has been discussed above. Okazaki teaches improvements in hot carrier reliability by the use of an MBN gate consisting "of a boron-doped and a nitrogen-doped (N-doped) poly-Si double layer" in which "[t]he N-doped Si layer is deposited on the gate oxide by LPCVD." (Page 2369, right column, Section II, first paragraph.) Okazaki at page 2370, top of right column, briefly mentions a forming gas sintering step, typically used during semiconductor device manufacture but which is not correlated in any way with improving hot carrier reliability, separately addressed by Okazaki's MBN gate structure. Mitani briefly mentions annealing, after source/drain electrode patterning, in "a nitrogen atmosphere containing 10% of hydrogen, thereby completing a transistor", again a typical "forming" process. Consequently, Mitani is seen to add nothing to Okazaki's own teaching and a person of ordinary skill in the art would have found nothing in Mitani to add to or change Okazaki's teaching.

Lisenker's deficiencies have been discussed above. Beyond that, Lisenker's proposal for addressing hot carrier issues is distinct from that taught by Okazaki and Lisenker does not suggest or provide any motivation for modifying Okazaki's own concept of obtaining hot carrier reliability improvement in a PMOS transistor in which hot carrier (hole) degradation problems dominate (see Abstract). In an n-channel device, to which claims 40, 62, 80 and 84 are more particularly directed, hot electron effects dominate. Considering the Examiner's hypothetical assertion, substitution of Lisenker's teaching for that of Okazaki would have rejected Okazaki's own explicit teaching and would have involved changing the principle of operation of Okazaki which is an impermissible basis for establishing a *prima facie* of obviousness. It is therefore urged that this rejection be withdrawn.

- Claims 40-48, 60-65 and 75-81 also have been rejected under 35 US 103 as unpatentable over IEEE Transactions on Nuclear Science, Vol. 39, No. 6, December 1992, pp. 2220-2229 (Saks) In view of Okazaki. Claims 42-46, 48, and 75 have been

cancelled making the rejection moot in respect of those claims. The rejection is respectfully traversed as to claims 40, 41, 47, 60-65 and 76-81.

Saks teaching, as discussed above in conjunction with Lisenker, is directed to the comparative effects of introducing deuterium and hydrogen into relatively thick MOSFET gate oxides by annealing samples in hydrogen and deuterium, respectively, "after definition of the polysilicon gates and implantation of the N+ source/drains", when the devices were subjected to ionizing gamma radiation. Saks concluded "There was essentially no effect on the pre-irradiation characteristics due to the 900°C D2/H2 annealing, either on the initial Dit value ... or the initial FET threshold voltages." (Page 2221, left column, Section II, second paragraph.) Thus, Saks teaching would have pointed a person of ordinary skill in the art away from the invention claimed in claims 40, 41, 47, 60-65 and 76-81.

Saks shows in Table 1 (page 2224) trap build up times for oxides annealed in H2 and D2, and the relative time retardation factor for the D2 oxide (Table 1, last column), showing retardation factors between 3.2 to 4.5 for D2 and noting "[b]ecause of the large +-25% experimental uncertainty, it is unclear how much of the measured variation is real." (Page 2224, right column, conclusion (1)). Thus, the isotope effect measured by Saks following deuterium annealing of a gate oxide prior to metalization is relatively insignificant. Ionizing irradiation following deuterium annealing of a gate oxide is a necessary ingredient of Saks' experiment but it has no relation to the invention claimed in claims 40, 41, 47, 60-65 and 76-81 of the present application and the disclosures by Saks and Lisenker would not have suggested or motivated the claimed invention.

Saks also discusses sintering in hydrogen " . . . which is normally the last moderately high temperature processing step after deposition of the aluminum metalization", i.e. the typical "forming" process discussed above. Saks sintered unannealed devices and devices having H2 annealed oxides in H2, and sintered devices having D2 annealed oxides in D2. Saks concluded: ". . . sintering had no discernable effect on the radiation sensitivity of any of the three oxide types." (Page 2222, right column, Section II D., third paragraph. Emphasis added.) Consequently, Saks teaches only that no significant changes on radiation sensitivity result in his experiments as between annealing in hydrogen and deuterium. Contrary to the Examiner's

assertion, Saks is not seen to disclose any degradation mechanism other than external irradiation and his teaching would not have suggested pertinence to MOS device degradation resulting from hot carrier effects during device operation, in particular hot electron effects, as disclosed in the present application and to the alleviation of which the invention claimed in claims 40, 41, 47, 60-65 and 76-81 of this application is directed.

In summary, Saks suggests that deuterium annealing prior to contact formation is no more effective than annealing in hydrogen, that such annealing followed by deuterium sintering after metalization produces insignificant benefits, and Saks does not teach or suggest effectiveness of deuterium annealing on device degradation due to hot carrier, in particular hot electron, effects, as discussed at page 3, line 12, et seq. of the specification of the present application.

The Examiner also asserts: "Saks teaches that transistors annealed in deuterium (D2) exhibit 3.2 to 4.5 fold retardation factor relative to transistors annealed in hydrogen (H2) (Saks, Table 1, page 2224)." Saks states that the estimated accuracy of the retardation factors in Table 1 is about +-25% and concludes because of this large experimental uncertainty it is unclear how much of the measured variation is real (Saks, page 2224, right column). This is about the same isotope mass effect as asserted by Lisenker (Lisenker, page 7, line 30 to page 8, line 12). In contrast, the specification of the present application discloses a typical isotope effect of 10 (page 22, line 21 to page 23, line 3) in a MOS device embodying the claimed invention. This enhanced isotope effect results from post gate contact deuterium annealing in combination with a thin gate insulator (not exceeding about 55 Angstroms) and there is no recognition or suggestion in the cited references of the desirability of such a combination of features nor of the problem solved and the benefits of reduced hot carrier (electron) degradation in a device embodying the invention.

Apart from the lack of relevance of Saks as discussed above, Saks does not suggest any motivation for rejecting and dispensing with (nor adding to) Okazaki's own teaching (discussed above in relation to Lisenker) to use an MBN gate consisting "of a boron-doped and a nitrogen-doped (N-doped) poly-Si double layer" in which "[t]he N-doped Si layer is deposited on the gate oxide by LPCVD." (Page 2369, right column, Section II, first paragraph.)

Existence of thin gate insulator devices were, per se, known at the time of the invention is not pertinent to the issue of patentability of claims 62 –65, and 76-81. What is pertinent is that there was no teaching or suggestion in the prior art that disclosed or would have suggested recognition of the desirability of, or the benefits to be obtained by, use of such a thin gate insulating layer in combination post gate contact annealing in deuterium to produce, in a device as claimed in this application, such a profound improvement in device degradation due to hot carrier effects, as evidenced by an isotope effect of 10 exemplified in Applicant's specification. Okazaki proposed a particular gate insulator structure to address hot hole degradation in a PMOS transistor and neither Lisenker nor Saks provides any motivation for that technique to have been rejected. Uchiyama et al. "High Performance Dual-gate Sub-halfmicron CMOSFETs with 6nm-thick Nitrided SiO2 Films in an N2O Ambient", IEDM Technical Digest, pp. 425-427, 1990 (cited in the accompanying Information Disclosure Statement) discusses 6nm gate oxide thickness CMOSFETs incorporating N2O nitrided gate dielectric films to block boron penetration and to reduce electron traps. Again, neither Lisenker nor Saks provides any motivation for that technique to have been rejected or modified.

Prima facie obviousness

The justifications asserted in the Office Action for motivation to combine references in the 35 US 103 rejections appear to be conclusory opinions lacking in factual support and reached without giving proper weight to the totality of teachings in the cited art considered as a whole. As the Examiner is aware, the fact that references could hypothetically be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of the combination. Even the existence of references that taught all individual aspects of a claimed invention is not sufficient to establish a *prima facie* case of obviousness without some objective reason in the prior art to combine the teachings of the references. Each reference must be considered as a whole in the light of the art at the time of the claimed invention, not on the basis of an arbitrarily selected feature of that particular reference - MPEP 2143.01. With respect, the Examiner has made no such factual showings suggested by the prior art. As demonstrated in the above discussion, not only do the references fail to disclose or suggest desirability for their combination in the manner asserted in the grounds of rejection, they do not, each considered as a whole, disclose, teach or suggest, all of the claim limitations in the

rejected claims (see MPEP 2143.03), but point away from the combinations of features set forth in claims 40, 41, 47, 60-65 and 76-81, each considered as a whole. Consequently, the grounds asserted in the Office Action are believed inadequate to sustain rejection of those claims under 35 US 103.

CONCLUSION:

It is believed this amendment and response addresses and overcomes all outstanding grounds of rejection, places all pending claims in condition for allowance, and satisfies the requirements for declaration of an interference with U.S. Patent 6,023,093. Favorable responsive action will be appreciated.

If after consideration, the Examiner believes that any outstanding matters remain, a telephone call to the undersigned attorney at 972-862-7428 will be appreciated.

Date: May 13, 2003

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Certificate of Facsimile Transmission under 37 CFR 1.8

In re Application No. . 09/160,657
Filed: September 25, 1998
Inventor: Joseph W. Lyding et al
For: Semiconductive Devices and Methods for Same

Group Art Unit: 2822
Attorney Docket: UIL-10013C
Examiner: VOCKRODT, Jeff B.

Fax No: 703-872-9318

I hereby certify that the below correspondence is being facsimile transmitted to the United States Patent Office on May 13, 2003.

- Amendment (15 pages).

(Signature)

N. Rhys Merrett

May 13, 2003
(Date)

PLEASE DELIVER TO:
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ART UNIT 2822
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RE: 09/160,657 Lyding et al

In response to your voice message, I am forwarding credit card charge authorization for the $84 excess claims fee. My apologies for the inadvertent error in fee calculation on my part.

Acknowledgment by fax of safe receipt will be appreciated.

Thank you.

N. Rhys Merrett

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